EXHIBIT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): JRI LEE and BEHZAD RAZAVI
Docket: G&C 30448.116-US-P1
Title: A 40-GB/S CLOCK AND DATA RECOVERY CIRCUIT IN 0.18MM CMOS TECHNOLOGY

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Enclosed herewith are the following application parts:

- ☒ Transmittal sheet, in duplicate, containing Certificate Of Mailing Under 37 CFR 1.10.
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- ☒ Verified statement to establish small entity status.
- ☒ Assignment of the invention to The Regents of the University of California, Recordation Form Cover Sheet.
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A 40-Gb/s Clock and Data Recovery Circuit in 0.18-μm CMOS Technology

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September 1, 2002

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Abstract

A 40-Gb/s CDR circuit incorporates a quarter-rate phase detector and a multiphase LC oscillator to retime the data and demultiplex it into four 10-Gb/s outputs. Fabricated in 0.18-μm CMOS technology, the circuit produces a clock jitter of 0.9 ps,rms and 9.67 ps,pp with a PRBS of $2^{31} - 1$ while consuming 144 mW.

Clock and data recovery (CDR) circuits operating at tens of gigabits per second pose difficult challenges with respect to speed, jitter, signal distribution, and power consumption. Half-rate 40-Gb/s CDR circuits have been implemented in bipolar technology [1, 2], but they require 5-V supplies and draw 1.6 to 5 watts of power. (The work in [1] uses an external oscillator and 90° phase shifter.) On the other hand, the recent integration of 10-Gb/s receivers in CMOS technology [3] encourages further research on CMOS solutions for higher speeds, especially if it enables low-voltage, low-power realization. This paper presents the design and experimental verification of a 40-Gb/s phase-locked CDR circuit fabricated in 0.18-μm CMOS technology.

A. CDR Architecture

Shown in Fig. 1, the circuit incorporates a multiphase voltage-controlled oscillator (VCO), a quarter-rate phase detector (PD), a voltage-to-current (V/I) converter, and a simple loop filter. The PD uses the half-quadrature phases provided by the VCO to sample the input data every 12.5 ps, thereby detecting data edges and determining whether the clock is early or late. Four of these samples fall in the center of the data eye, retiming and demultiplexing the 40-Gb/s input into four 10-Gb/s outputs. In the absence of data transitions, the V/I converter generates no output current, leaving the oscillator control line undisturbed. The circuit is fully differential, except for the oscillator control line. With quarter-rate sampling, the flipflops' hold time can be four times as long as that required in full-rate operation, but their acquisition speed must still guarantee correct sampling of the input bits in less than 25 ps.

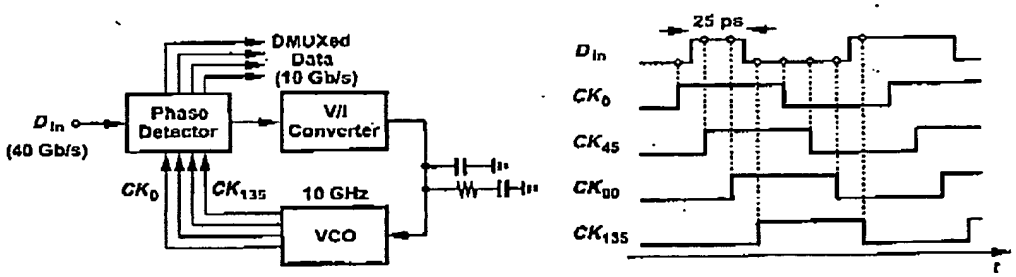


Fig. 1. CDR architecture.

B. *Building Blocks*

VCO The speed, jitter, and driving capability required of the oscillator point to the use of an LC realization. A number of multiphase LC oscillators have been reported. Coupled oscillators [4, 5] operate away from the resonance frequency of the tanks so as to create the required phase shift, thus bearing a trade-off between reliability of oscillation and the phase noise [5]. Furthermore, such topologies are prone to oscillation at more than one frequency because they can satisfy gain and phase requirements at multiple frequencies. The multiphase oscillator in [6] drives transmission lines by a gain stage loaded by resistors, incurring energy loss in each cycle.

The multiphase oscillator introduced here is based on the concept of differential stimulus of a closed-loop transmission line at equally-spaced points. Illustrated in Fig. 2, the circuit sustains a phase separation of 180° at diagonally-opposite nodes, providing 45° phase steps in between. Unlike the topologies in [5] and [7], this circuit does not operate away from the resonance frequency. Moreover, its oscillation frequency is uniquely given by the travel time of the wave around the loop. Also, in contrast to the design in [6], the transmission line requires no termination resistors, thereby displaying lower phase noise and larger voltage swings for a given power dissipation and inductor Q.

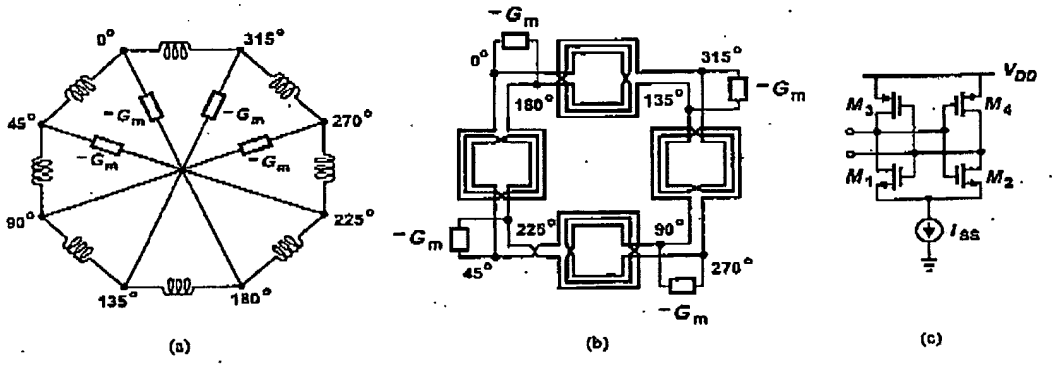


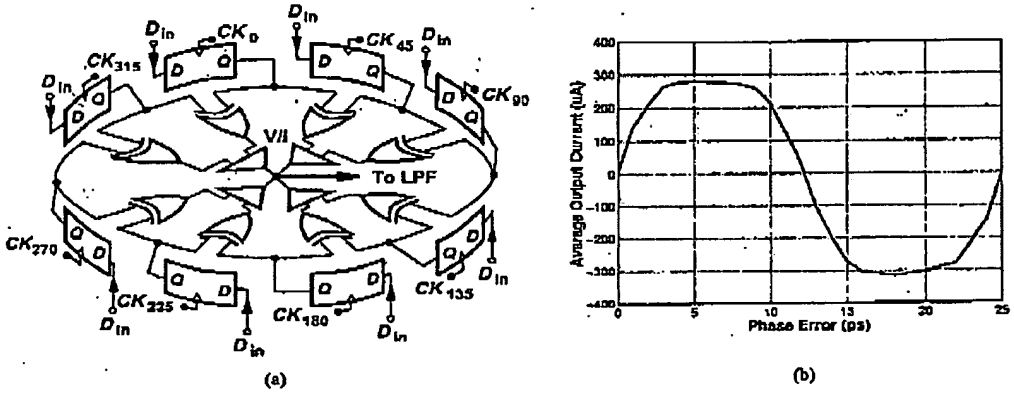
Fig. 2. (a) Proposed half-quadrature oscillator, (b) modification of (a), (c) realization of $-G_m$ cell.

The topology of Fig. 2(a) nonetheless necessitates long interconnects between the nodes and their corresponding $-G_m$ cells. However, recognizing that diagonally-opposite inductors carry currents that are 180° out of phase, we modify the circuit as shown in Fig. 2(b), grouping inductor elements into differential structures and placing the $-G_m$ cells in close proximity of the oscillator nodes. Exploiting the higher Q of differential inductors [8], the VCO incorporates the $-G_m$ cell

shown in Fig. 2(c), shaping the rising and falling edges by the PMOS transistors and hence lowering the upconversion of $1/f$ noise [9]. SpectreRF simulations indicate that, for a given power dissipation, inductor Q, and frequency of oscillation, the proposed oscillator achieves twice the voltage swings and 12 dB lower phase noise than that in [6].

Each differential port of the VCO is buffered by an inductively-loaded differential pair. These buffers (1) isolate the VCO from the long interconnects going to the PDs that would otherwise introduce greater uncertainty in the oscillation frequency; (2) generate voltage swings above the supply voltage, thus driving the flipflops efficiently; (3) isolate the VCO from the data edges coupled through the phase detectors.

Phase Detector The PD employs eight flipflops to strobe the data at 12.5-ps intervals [Fig. 3(a)]. In a manner similar to an Alexander topology [10], the PD compares every two consecutive samples by means of an XOR date, generating a net output current if the two are unequal, i.e., if an edge has occurred. With no data transitions, the FFs produce equal outputs, and the V/I converters a zero current.



(a) (b)

Fig. 3. (a) Quarter-rate phase detector, (b) its characteristic.

The early-late phase detection method used here exhibits a bang-bang characteristic, forcing the CDR to align every other edge of the clock with the zero crossings of data under the locked condition. In reality, the metastable behavior of the flipflops leads to a finite PD gain, allowing the clock edges to sustain some offset with respect to the data zero crossings. Shown in Fig. 3(b) is the input/output characteristic of the PD together with the V/I converter, obtained by transistor-level simulations while the circuit senses a 40-Gb/s random data stream and eight phases of the 10-GHz

clock. For a phase error less than ±2.5 ps, the PD displays a relatively constant gain of 100 μA/ps. With an ideal V/I converter, a finite phase difference, $\Delta\phi$, would still lead to injection of a finite current into the loop filter (similar to an ideal integrator), forcing the CDR circuit to lock with zero static phase error. The output resistance of the V/I converter, on the other hand, results in lossy integration, necessitating a small change in $\Delta\phi$ as the control voltage varies from minimum to maximum.

Even though the PD flipflops operate with a 10-GHz clock, proper sampling of 40-Gb/s data still requires fast recovery from the previous state and rapid acquisition of the present input. To this end, both a wide sampling bandwidth and a short clock transition time are necessary. Figure

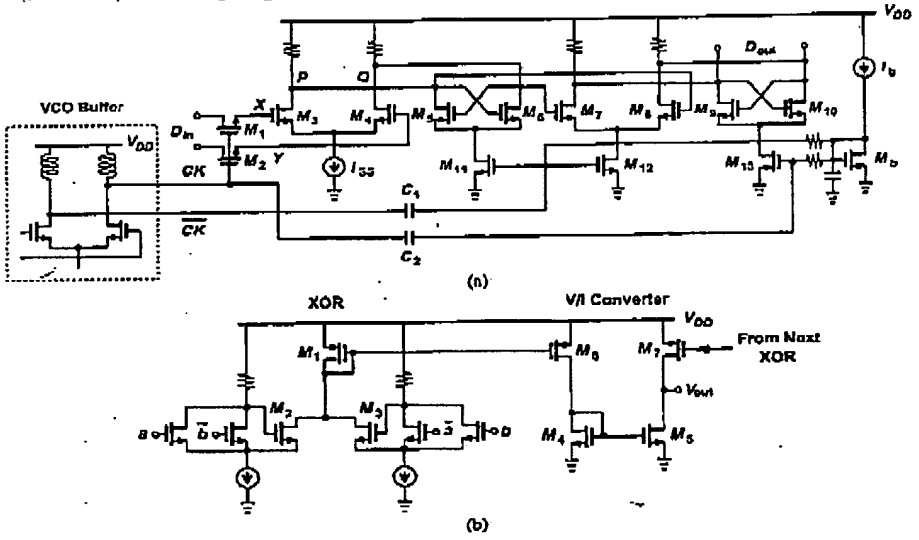


Fig. 4. (a) Proposed flipflop, (b) symmetric XOR gate and V/I converter.

4(a) depicts the master-slave flipflop used in the phase detector. Here, NMOS switches M_1 and M_2 sample D_{in} on the parasitic capacitances at nodes X and Y when CK is high. Since the minimum input common-mode (CM) level is dictated by the gate-source voltage of M_3-M_1 and the headroom required by I_{SS}, the sampling switches experience only an overdrive voltage of 0.5 V even if CK reaches V_{DD}, failing to provide fast sampling. This issue is remedied by setting the CM level of CK and $\overline{CK}$ equal to V_{DD}, a choice afforded by inductively-loaded stages following the VCO core. The peak value of CK thus exceeds V_{DD} by 0.8 V, more than doubling the sampling speed of M_1 and M_2. The large clock swings also minimize the transition times.

With large clock swings available, the current switching in pairs M_5-M_6, M_7-M_8 and M_9-M_{10} is accomplished by gate control rather than conventional source-coupled steering. The proposed topology offers two advantages: (1) since the tail current source is removed, M_{11}-M_{13} can be quite narrower, presenting a smaller capacitance to the VCO buffer; (2) since the drain currents of M_{11}-M_{13} are not limited by a tail current source, these transistors experience "class AB" switching, drawing a large current at the peak of the clock swing and providing greater voltage swings and a higher gain in the data path.

The XOR gates used in the PD must exhibit symmetry with respect to their two inputs and operate with a low supply voltage. Shown in Fig. 4(b) along with the V/I converter, the XOR gate is a modified version of that in [11], with transistors M_2 and M_3 forming local positive feedback loops and avoiding the reference voltage necessary in the realization in [11]. The V/I converter copies the output current of the XOR, providing nearly rail-to-rail swings for the oscillator control line.

C. *Experimental Results*

The CDR circuit has been fabricated in a 0.18-μm CMOS technology. Figure 5 shows a photo of the die, which measures $1.0 \times 1.4\ mm^2$. The circuit is tested on a high-speed probe station with a 40-Gb/s Anritsu random data generator providing the input.

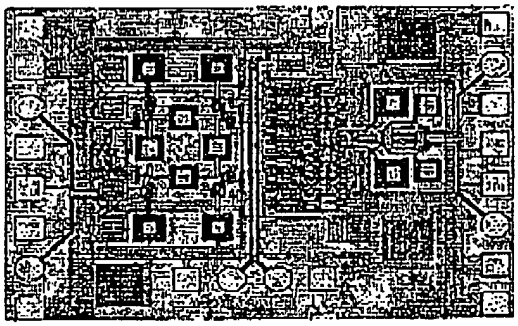


Fig. 5. Chip micrograph.

Shown in Fig. 6 are the VCO tuning characteristic and free-running spectrum. The VCO provides a tuning range of 1.2 GHz with a free-running phase noise of -105 dBc/Hz at 1-MHz offset. Figure 7(a) depicts the CDR input and output waveforms under locked condition in response

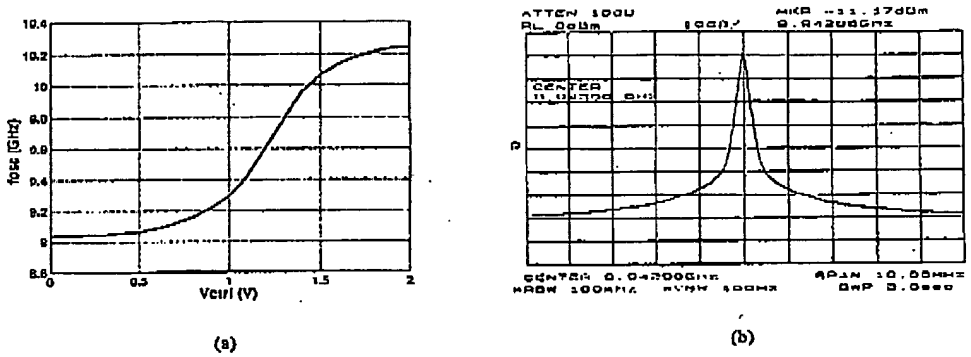


Fig. 6. (a) VCO tuning range, (b) free-running spectrum.

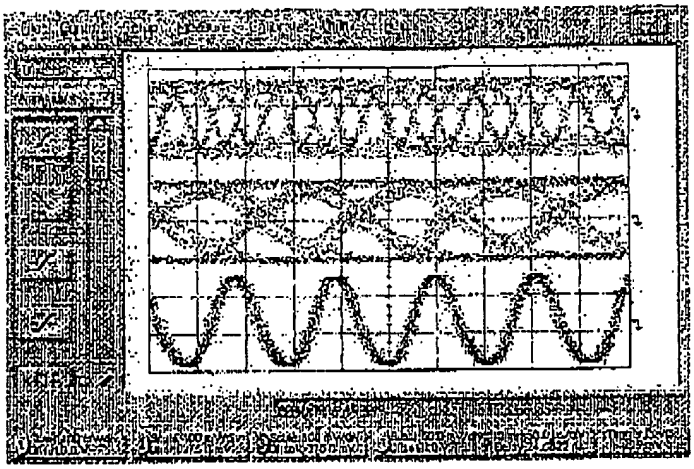
	[1]	[2]	[6]	This Work
Input Data Rate	40 Gb/s	40 Gb/s	10 Gb/s	40 Gb/s
Output Data Rate	2 x 20 Gb/s	4 x 10 Gb/s	2 x 5 Gb/s	4 x 10 Gb/s
Rec. Clock Jitter	0.8 ps,rms	0.7 ps,rms	1.2 ps,rms	0.9 ps,rms
Power Diss.	1.6 W	4.3 W	360 mW	144 mW
Supply Voltage	5 V	5 V	1.8 V	2 V
Area	0.9 mm x 0.9 mm	3 mm x 3 mm	1.9 mm x 1.5 mm	1.0 mm x 1.4 mm
Technology	50-GHz Bipolar (Uses external VCO & divider)	72-GHz SiGe	0.18-um CMOS	0.18-um CMOS

Table 1. CDR performance summary.

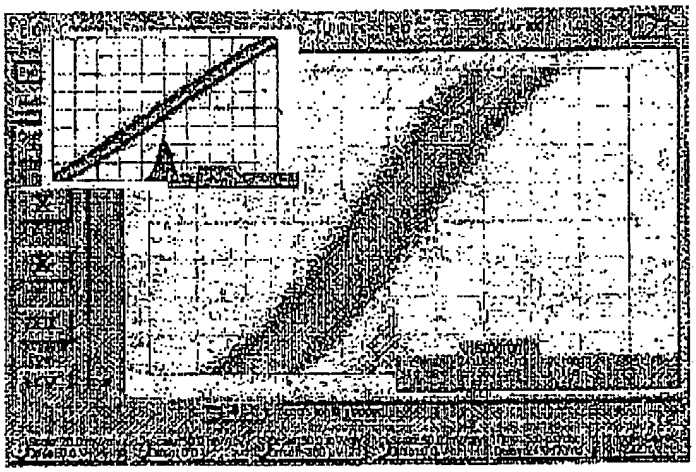
to a pseudo-random sequence of length $2^{31} - 1$. The demultiplexed data experiences some ISI, but if further demultiplexing is included on the same chip, the ISI can be tolerated. Figure 7(b) shows the recovered clock, suggesting an rms jitter of 1.756 ps and a peak-to-peak jitter of 9.67 ps. However, as shown in the inset, the oscilloscope itself suffers from rms and peak-to-peak jitters of 1.508 ps and 8.89 ps, respectively. Thus, the CDR output contains a jitter of 0.9 ps,rms and at most 9.67 ps,pp. [1] The proformance of this work and some other previously-published CDR circuits is summarized in Table 1. [2]

[1] It is unclear whether and how the peak-to-peak values can be subtracted.

[2] The power dissipation noted here for the design in [2] excludes their limiting amplifier and frequency detector contribution and was obtained through private communication with M. Reinhold.



(a)



(b)

Fig. 7. (a) Top to bottom: input data, one demultiplexed output data, and recovered clock (horizontal scale: 50 ps/div, vertical scale: 100 mV/div), (b) clock jitter measurement (horizontal scale: 5 ps/div for both histograms).

REFERENCES

[1] M. Wurzer et al, "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silicon Bipolar Technology," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1320-1324, Sept. 1999.

[2] M. Reinhold et al, "A Fully Integrated 40-Gb/s Clock and Data Recovery IC with 1:4 DEMUX in SiGe technology," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1937-1945, Dec. 2001.

[3] J. Cao et al, "OC-192 Receiver in Standard 0.18μm CMOS," *ISSCC Dig. Tech. Papers*, pp. 250-251, Feb. 2002.

[4] J. Kim and B. Kim, "A Low Phase-Noise CMOS LC Oscillator with a Ring Structure," *ISSCC Dig. of Tech. Papers*, pp. 430-431, Feb. 2000.

[5] T. P. Liu, "A 6.5 GHz Monolithic CMOS Vlotage-Controlled Oscillator," *ISSCC Dig. of Tech. Papers*, pp. 404-405, Feb. 1999.

[6] J. E. Rogers and J. R. Long, "A 10-Gb/s CDR/DEMUX with LC Delay Line VCO in 0.18μm CMOS," *ISSCC Dig. of Tech. Papers*, pp. 254-255, Feb. 2002.

[7] J. Savoj and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection," *ISSCC Dig. Tech. Papers*, pp. 78-79, Feb. 2001.

[8] M. Danesh et al., "A Q-Factor Enhancement Technique for MMIC Inductors," *Proc. IEEE Radio Frequency Integrated Circuits Symp.*, pp. 217–220, April 1998.

[9] A. Hajimiri and T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," *IEEE Journal of Solid-State Circuits*, pp. 179-94, Feb. 1998.

[10] J. D. H. Alexander, "Clock Recovery from Random Binary Data," *Electronics Letters*, vol. 11, pp. 541-542, Oct. 1975.

[11] B. Razavi et al, "Design Techniques for Low-Voltage High-Speed Digital Bipolar Circuits," *IEEE Journal of Solid-State Circuits*, pp. 332-9, March 1994.

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DATE: 7 February 2007

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Applicant(s): JRI LEE and BEHZAD RAZAVI
Serial No.: Not yet assigned
Filed: Herewith
For: A 40-Gb/s Clock and Data Recovery Circuit in 0.18-mm CMOS Technology
Group: Not yet assigned
Examiner: Not yet assigned

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